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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PORTKA, GARY J	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/584,301	HELMS, FRANK P.	
	Examiner	Art Unit	
	Gary J Portka	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-27 and 31-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-27 and 31-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 9, and 21 have been amended, and claims 8, 28-30, and 34 have been canceled by Applicant. Claims 1-7, 9-27, and 31-33 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 23, 26-27 and 32-33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 23, 26 and 32 substantially recite the memory control signal is controlled from a first region in an integrated circuit during an operational state, and from another location in the integrated circuit during a power savings state. Applicant's disclosure does not appear to show the memory control signal controlled in both states from a single integrated circuit. These claims are apparently directed to the embodiment shown in Fig. 7. Since the memory controller 704 controls the signal in the operational state, and since 704 loses power in the power savings state, it must be that the signal is controlled by I/O hub 709, via signal 708, in this state. The logic at 707 does not control the signal, but merely passes it, and it does so in both states. Claims 27 and 33 incorporate this limitation by dependency.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-7 and 13-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1 and 14 recite that the other location or second circuit is independent of the first integrated circuit or memory control circuit, further in claim 1 during normal operation. The intended scope of the limitation "independent" is unclear from the specification. It may be generally argued that since the relevant circuits are a part of the same system, they are interdependent. It may be more specifically argued that since the relevant circuits control the memory control signal exclusively of one another, they are interdependent (one cannot control while the other controls). Claims 2-7, 13, and 15-20 incorporate this limitation by dependency.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-7, 9, 14-15, 17, 19-20, 26, and 31-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Baweja et al., US 6,212,599 B1.

8. As to claims 1-7, 14, 19-20, Baweja discloses *a method for and computer system controlling a self refresh state of memory, comprising supplying a memory control signal*

(CKE 330, Fig. 3) *to the memory from a first integrated circuit* (210, Fig. 2) *according to an operational state* (first operation mode, via SDCKE 240 and 320, Fig. 3), *supplying the memory control signal from another location* (310, Fig. 3) *when in a power savings state to maintain the self refresh state* (via SCKE and 320, Fig. 3), *the other location* (310) *independent of the first integrated circuit* (210) *during normal operation* (state machine 310 is not affected by and does not otherwise interact with first memory controller 210). See Abstract, Figs. 2-3, col. 2 line 40 to col. 2 line 5, col. 4 lines 23-28, and col. 4 line 64 to col. 5 line 22.

9. As to claims 9, 15, and 17, Baweja discloses the claimed invention substantially as described above with regard to claims 1 and 14. The limitation that the first integrated circuit is isolated from the memory during the power savings state, by disabling a switch coupling them is met by the AND gate 320 coupling to the CKE 330 signal. That is, when first state machine 310 outputs low SCKE (the recited switch enable signal that turns off the switch) in response to going into sleep mode, CKE 330 remains low regardless of state of the first integrated circuit output SDCKE 240, effectively isolating SDCKE and disabling it's connection to CKE.

10. As to claims 26 and 31-32, Baweja discloses the claimed invention substantially as described above with regard to claims 1 and 14. The limitation that the signal that holds the control signal is an asserted reset signal is met by the SCKE signal of Baweja, since SCKE low may be considered asserted.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 10-13, 16, 18, and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baweja et al., US 6,212,599 B1, in view of AMBA Interconnection Schemes, Application Note 05, ARM DAI 0005A, 1998.

13. As to claims 10-13, 16, 18, and 21-25, Baweja discloses the claimed invention substantially as described hereinabove, but does not disclose that the other location drives the output at high impedance during the operational state. In Baweja a choice is made of how to make CKE to the memory low when either of SDCKE from the first memory controller or SCKE from the first state machine are low, and the solution made is to use an AND gate. However, a more fundamental view of the problem is simply how to connect the two inputs SDCKE and SCKE to control CKE as desired. As taught by the AMBA Interconnection reference, there are various methods known of connecting multiple sources to multiple destinations. These methods clearly apply for multiple sources to one destination as well, since no modifications are mentioned at the destinations. As described at pages 1-2 through 1-3, and at 3-2, a tristate bus implemented using tristate drivers avoids the requirement for external switches or gates, providing connection through a single wire, and therefore might be easier to implement due to space or cost savings. A tristate driver output of an unused source is driven to

high impedance as recited. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to drive an output at high impedance as recited, because this would result from the use of a tristate driver to make the connections, such drivers known to allow multiple connections while preventing the requirement for external gates and switches.

14. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baweja et al., US 6,212,599 B1, in view of Henkhaus et al., US 6,654,895 B1.

15. As to claim 27, Baweja does not disclose a S3 suspend to RAM state. However, this state was previously known in the art. See Henkhaus col. 1 lines 57-65, which describe the S3 state as cutting all power except that to save system memory, and that this state is ideal to achieve an instantly available computer since it saves the most power while allowing fast restart. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use this state, because it was a known state to achieve maximum power savings while still allowing fast restart.

16. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baweja et al., US 6,212,599 B1.

17. As to claim 33, Baweja does not disclose the integrated circuit includes the memory control circuit and the CPU. However, it has long been known in the art that the combination of elements into fewer elements, such as integration of a plurality of elements into a single chip, has benefits of lowering cost and a possible improvement in speed due to smaller circuit scale. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to integrate the memory controller and CPU on

the same circuit, because of the long known benefits from integration of lower cost, space requirements, and possible improved performance.

Response to Arguments

18. Applicant's arguments filed November 30, 2004, and in the brief filed May 24, 2004 have been fully considered but they are not persuasive. Applicants have argued that in Baweja the signal CKE 330 is supplied from the same location during both states. However, even if respective sources 210 and 310 are a part of the memory system controller 200, this does not change that the sources are in different locations to the extent claimed. Applicant argues that Baweja no reset signal as claimed, but as discussed above the low SDCKE signal meets the claim limitations required for the reset signal. Applicant argues that Baweja does not isolate the first circuit with a switch, but as discussed above isolation occurs when changing the first circuit input to the gate causes no change in the output, and since it is so isolated those transistors of the gate have performed the function of the switch to the extent claimed. Applicant argues that in Baweja the second location is not independent of the first since it is part of the same memory controller. Examiner does not agree to the extent understood; all computer system elements may be said to be a part of the same computer system, and yet Applicant would probably agree that some items within are independent of each other. Examiner clarifies that the second location is considered the state machine 310, which equivalently amounts to the considering of gate 320 as being outside the first and second locations, and thus the first and second locations are independent as recited.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Patent No:

5,940,851 DRAM refresh with external or internal clock (Fig. 3).

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary J Portka
Primary Examiner
Art Unit 2188

March 8, 2005